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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,954	07/11/2001	Hagen Eckert	4100-0127P	6066

2292 7590 04/11/2007  
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EXAMINER
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ODOM, CURTIS B

ART UNIT	PAPER NUMBER
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2611

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/11/2007	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/11/2007.

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mailroom@bskb.com

JK

<b>Office Action Summary</b>	<b>Application No.</b> 09/856,954	<b>Applicant(s)</b> ECKERT, HAGEN	
	<b>Examiner</b> Curtis B. Odom	<b>Art Unit</b> 2611	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 February 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 5-7, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Suominen et al. (previously cited in Office Action 6/13/2006), and in further view of Nishimura (previously cited in Office Action 1/11/2006).

Regarding claim 1, applicant discloses as prior art an arrangement (Fig. 1) for measurement demodulation and modulation error measurement of a digitally modulated receive signal, with a receive filter (Fig. 1, block 1), and a following demodulator (Fig. 1, block 2) for frequency and phase error compensation (section 0004) for determining ideal symbol samples, wherein measuring signals are output from the demodulator and the error correction stage (substitute specification, section 0004 and 0006).

wherein a first measuring signal is filtered in a reference filter (Fig. 1, block 13, section 0004) and a second measuring signal is filtered using a weighting filtered function (Fig. 1, block 11, section 0006) in accordance with the ETSI specification, the first measuring signal and the second measuring signal are then evaluated in a following evaluation circuit (Fig. 1, block 4, section 0006), and

wherein the second measuring signal of the demodulator output from the error correction stage is filtered in a weighting filter equivalent to a measuring filter (Fig. 1, block 11, section 0006).

The applicant does not disclose the weighting filter function is formed by cascaded filter functions of the receive filter and the weighting (measuring) filter and the demodulator is directly between the receive and measuring filters.

However, Suominen et al. discloses coefficients used for weighting in a filter are a result of a weighting filter function which involves the convolution of two individual filters (functions) (see column 7, lines 5-17). Suominen et al. further discloses that two filters can be cascaded into one filter by convolution of the impulse responses (filter functions) of each individual filter (column 7, lines 5-17). Therefore, it would have been obvious to one skilled in the art at the time the invention was made that since the applicant discloses the weighting (measuring) filter can be designed in accordance with a desired filter function (section 0006) to modify the weighting (measuring) filter of the applicant with cascading filter functions of the receive filter and weighting (measuring) filter as disclosed by Suominen et al. to obtain a filter with increased functionality which can perform two filtering operations within one filter (see Suominen et al., column 7, lines 5-17).

Nishimura further discloses a demodulation unit which includes error correction of a digitally modulated signal (Abstract and column 4, lines 32-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the error correction stage as disclosed in the admitted prior art could have been eliminated by incorporating the error correction in the demodulator in the same manner as taught by Nishimura since implementing the error correction in the demodulator would decrease the size of the hardware and allow for simpler implementation since there would be less separate hardware components. This incorporation would allow the weighting filter to receive the first measuring directly from the demodulator and the demodulator to be implemented directly between the receive and measuring filter.

Regarding claim 2, which inherits the limitations of claim 1, Suomminen et al. further discloses the filtering function of the single filter is determined by the convolution operation relationship of two cascaded filter functions (column 7, lines 5-17). It would have been obvious to include this feature to obtain a filter with increased functionality which can perform two filtering operations within one filter (see Suominen et al., column 7, lines 5-17).

Regarding claim 3, which inherits the limitations of claim 1, applicant discloses as prior art the receive filter is designed according to the requirements of the demodulator for supplied signal characteristics (section 0004), wherein matched filter is designed in accordance with the requirements of the demodulator for supplied signal characteristics (see section 0015).

Regarding claim 5, applicant discloses as prior art an arrangement for measurement demodulation and modulation error measurement of a digitally modulated signal, the arrangement comprising:

a receive filter (Fig. 1, block 1, section 0004) for receiving the digitally modulated signal and for filtering the digitally modulated signal;

a demodulator (Fig. 1, block 2, section 0004) for receiving the filtered digitally modulated signal from the receive filter, for performing phase and frequency error correction and outputting a first measuring signal to an error correction stage (Fig. 1, block 10, sections 0004 and 0006), and for determining ideal symbols (section 0004) from the first measuring signal, and outputting a second measuring signal to a reference filter (Fig. 1, block 13);

a reference filter (Fig. 1, block 13, section 0004) for receiving the second measuring signal from the demodulator and for filtering the second measuring signal;

a weighting (measuring) filter (Fig. 1, block 11, section 0006) for receiving the first measuring signal from the error correction stage for weighting filtering the first measuring signal; and

an evaluation circuit (Fig. 1, block 4, section 0006) for evaluating the filtered second measuring signal from the reference filter and the weighting filtered first measuring signal from the measuring filter,

The applicant does not disclose that the weighting filter function is formed by cascaded filter functions of the receive filter and the measuring filter and error compensation performed to produce the first measuring signal is eliminated or performed internally in the demodulator so that the demodulator is implemented directly between the receive and measuring filters.

Suominen et al. further discloses coefficients used for weighting in a filter are a result of a weighting filter function which involves the convolution of two individual filters (functions) (see column 7, lines 5-17). Suominen et al. further discloses that two filters can be cascaded into

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one filter by convolution of the impulse responses (filter functions) of each individual filter (column 7, lines 5-17). Therefore, it would have been obvious to one skilled in the art at the time the invention was made that since the applicant discloses the weighting (measuring) filter can be designed in accordance with a desired filter function (section 0006) to modify the weighting (measuring) filter of the applicant cascading filter functions of the receive filter and weighting (measuring) filter as disclosed by Suominen et al. to obtain a filter with increased functionality which can perform two filtering operations within one filter (see Suominen et al., column 7, lines 5-17).

Nishimura further discloses a demodulation unit which includes error correction of a digitally modulated signal (Abstract and column 4, lines 32-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the error correction stage as disclosed in the admitted prior art could have been eliminated by incorporating the error correction in the demodulator in the same manner as taught by Nishimura since implementing the error correction in the demodulator would decrease the size of the hardware and allow for simpler implementation since there would be less separate hardware components. This incorporation would allow the weighting filter to receive the first measuring directly from the demodulator and the demodulator to be implemented directly between the receive and measuring filter.

Regarding claim 6, Suominen et al. further discloses the filtering function of the single filter is determined by the convolution operation relationship of two cascaded filter functions (column 7, lines 5-17). It would have been obvious to include this feature to obtain a filter with

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increased functionality which can perform two filtering operations within one filter (see Suominen et al., column 7, lines 5-17).

Regarding claim 7, the applicant discloses as prior art the receive filter is designed according to the requirements of the demodulator for supplied signal characteristics (section 0004), wherein matched filter is designed in accordance with the requirements of the demodulator for supplied signal characteristics (see section 0015).

Regarding claim 9, applicant discloses as prior art the reference filter receives the second measuring signal directly from the demodulator (Fig. 1, block 13, page 1, lines 33-39 of the instant specification). The applicant does not specifically disclose as prior art that the measuring (weighting) filter receives the first measuring signal directly from the demodulator. However, the applicant does disclose as prior art that the measuring (weighting) filter receives the first measuring signal directly from an error correction stage. Nishimura further discloses a demodulation unit which includes an error correction stage to correct errors of a digitally modulated signal (Abstract and column 4, lines 32-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the demodulator disclosed as prior art could have also incorporated the error correction disclosed in the prior art in the same manner as taught by Nishimura since implementing the error correction in the demodulator would decrease the size of the hardware and allow for simpler implementation since there would be less separate hardware components. This would allow for the first measuring signal to be directly received from the demodulator.

Regarding claim 10, the claimed method includes features corresponding to the above subject matter mentioned in the rejection of claim 5 which is applicable hereto.



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4. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view Suominen et al. (previously cited in Office Action 6/13/2006) and in view of Nishimura (previously cited in Office Action as applied to claim 1/11/2006) as applied to claims 1 and 5, and in further view of Tsuda (previously cited in Office Action 1/11/2006).

Regarding claims 4 and 8, applicant's admitted prior art, Suominen et al., and Nishimura disclose all the limitations of claim 4 except the receive filter is designed so that ISI-free samples are fed to the demodulator.

Tsuda discloses a filter which receives a modulated digitally modulated signal designed so that ISI-free samples are fed to a demodulator (column 6, lines 10-21). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the receive filter of the applicant's admitted prior art, Suonminen et al., and Nishimura with the teachings of Tsuda and remove ISI from the samples before the demodulation since ISI can cause a loss of information during processing of the signal.

### ***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A handwritten signature in black ink, appearing to read 'Curtis Odom', with a stylized flourish extending from the end.

Curtis Odom

April 2, 2007